signal integrity

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"… detailed simulation and validation are necessary to guarantee a successful design"

The last decade has seen huge changes for PCB design bureaus such as Advanced Layout Solutions (ALS). What was once considered a 'board' for connecting together components has now become one of the most critical components in its own right. Our customers' needs have continually shifted as clock speeds and edge rates have steadily increased, taking PCB design from a drawing office post-process to an engineering activity at the heart of the design itself. Indeed, many product designs today don't even get off the ground until some sort of pre-route simulation has been completed to assess what is feasible from the chip IOs and PCB interconnect. For the PCB layout bureau, this change in bias must be understood. An increasing number of customers are experimenting with their own pre-route simulations to get up-front guidance as to how a product should be designed. However, many are finding this approach troublesome. If a signal is enough of a concern to be simulated then it should be done as accurately as possible. Entry-level signal integrity (SI) software packages use ideal lossless transmission lines and can only cope with simulating simple, single-trace topologies, making them inadequate for high-speed signalling and identifying crosstalk constraints on interconnect. High-end simulators will model frequency-dependant phenomena *(skin-effect, dielectric heating, etc.)* but require serious investment in tools and training, often too much investment for only occasional use.

A recent survey indicated that more than half of our customers were using PCB interconnect at over 300Mbps, with over a third above 1Gbps. As more and more designs go high-speed, it's fast becoming a necessity to thoroughly simulate the layout, ensuring the interconnect has sufficient bandwidth to distribute these signals without excessive distortion.

But what is *high-speed?*

It is a question that comes up time and again. High-speed is not an absolute clock frequency or edge-rate, rather it is a point where we must amend our design process to ensure that we are looking after the correct parameters. As interface trends constantly change, so too do the critical design parameters applicable to that technology. A high-speed parallel bus structure will require tight trace length constraints to control timing. However, in emerging high-speed serial standards the skew between differential pairs is pretty much ignored, it is now transmission line losses and impedance continuity that are the key constraints (*in stark contrast to parallel buses being matched to within a few picoseconds, PCI-Express™ recommends all lanes need only be matched to within half a nonosecond!*). The bottom line is that, irrespective of your data rate, if confidence is low then there's a strong case for running simulations.

What does ALS have to offer?

Advanced Layout Solutions is focused on Cadence Design Systems' Allegro PCB platform, and is the only design bureau to have incorporated signal integrity tools into the PCB design flow. Allegro PCB SI™ (formerly known as SPECCTRAQuest™) is a signal integrity version of the state-of-the-art Allegro PCB tool and provides vital layout guidance and verification at all stages of the design process. SI is a broad subject, straddling digital and analogue design, and in the context of our PCB design environment we now heavily rely on the SI tools for the following tasks:

- **Pre and post-route simulation**
- **Constraint management**
- **Stack-up & materials**
- **SI design audits**

Pre-route simulation

We offer access to the SI tools at the pre-route stage for product feasibility studies. This type of analysis includes exploratory simulations to evaluate topologies, identify design constraints and determine stack-ups.

Fig1. The SignalXplorer canvas modelling a three lane PCI-Express™ System.

We can evaluate IO capabilities and determine trace lengths, impedances, termination values etc. In this '*what if?*' stage of design the 'SignalXplorer canvas', shown in Fig1, makes it extremely easy to link up interconnect and driver models to quickly get experimenting and evaluating ideas. If a concept isn't going to work, now is the time to find out!

Constraint management

Failing to constrain routing can lead to failure, while over-constraining can make routing impossible to design. Pre-route simulation allows us to develop constraints that are appropriate for the interconnect, striking a balance between what is necessary and what is practical.

*Fig2. The embedded **Constraint Manager** ensures both physical and electrical rules are met.*

There is an endless list of electrical constraints available to the design engineer, from overshoot (mV) to first switch times (ns). It is the purpose of constraint-driven design to first identify what's required from a layout, and to then quickly meet those requirements.

Post-route simulation

Once a design is complete an enormous amount of data can be generated and reported back to our customers. Whether the layout came from the Cadence or Mentor design flow, we can provide extensive simulation reports that form a 'sign-off' status for the finished design files, detailing parameters from crosstalk voltage to propagation delay. What looked good in pre-route analysis may not look so good once the *actual* routing is analysed. In post-route simulation we can verify that our strategy has worked and ensure that we're not likely to suffer from unforeseen effects caused by vias and interconnect.

What about MGHz serial links?

With 3.125Gbps transceivers now readily available in off-the-shelf FPGAs (such as Xilinx's RocketIO™ and Altera's high-speed SERDES IO), it's no surprise that we are seeing an increasing number of customers integrating this technology into their designs. But for a serial link to work correctly requires the transmission medium be carefully designed. Impedance mismatch, incorrect termination and poor differential pair phase control are all factors that can prevent the receiver extracting the data correctly. Using Allegro PCB SI™ Advanced Layout Solutions is able to accurately model MGHz links by using transistor-level HSPICE® transceiver models - *(don't even think about looking for an IBIS model: serial transceivers have data-dependant output characteristics such as 'pre-emphasis' which places them well out of the reach of the IBIS specification).* These verified models have been correlated to match both the actual silicon design and empirical data, giving engineers the ability to design, simulate, and implement multi-gigabit data channels that are free from board-level signal quality issues. The combination of Allegro PCB SI™ and Synopsys' HSPICE® simulator provides the route to successful implementation of third generation serial connectivity standards such as PCI-Express™, Serial RapidIO™, Gigabit Ethernet and InfiniBand™.

This is an extract from the PCI-Express™ specification, and is a phrase that's fast becoming common in component datasheets and design guides:

"…detailed simulation and validation are necessary to guarantee a successful design".

SI design audits

Another service that customers find beneficial is the design audit. In this scenario we will take an existing design (or functional block of a design) and combine simulation results with the component datasheets to ensure the finished system meets specification. Here we'll be looking for signal integrity issues and timing violations as well as more general design factors such as return current consideration, decoupling strategy, etc. When a problem is identified SignalXplorer can be used as a 'virtual debug' tool whereby simulation can reveal the corrective action required, which may involve a PCB change or simply a component modification.
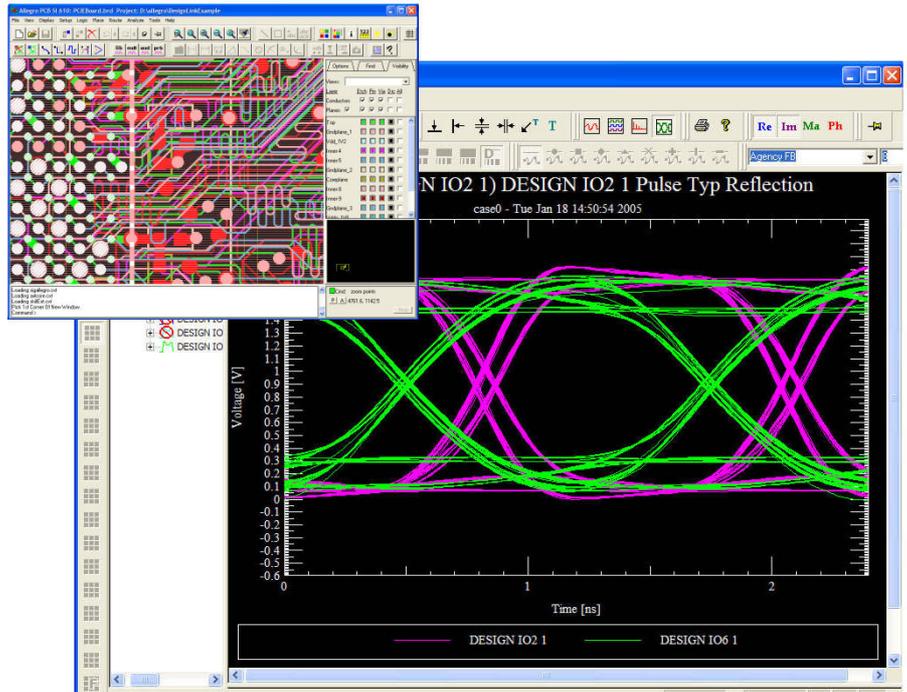
Viewing the results of simulation in **SigWave** *is the natural way to study signals. Waveforms can be viewed in the time or frequency domain and eye patterns allow us to view signals in exactly the way we would on an oscilloscope or serial data analyser. Furthermore, data can be imported from Tektronics, LeCroy, Hewlett-Packard and Agilent laboratory instruments, allowing us to complete the loop and simultaneously display simulated and actual waveforms at the end of the design.*

Where interconnect technology goes from here is anybody's guess. That said, it's highly unlikely that successful PCB designs are going to become any easier to achieve, especially without the use of board-level simulation…

Simulation capabilities

- IBIS 2.1, 3.2, 4.0, DML and encrypted HSPICE® model support for IOs
- Advanced field-solver models frequency-dependant crowding phenomena (Dielectric loss, skin effect and proximity effect all taken into account)
- Coupled trace models for crosstalk simulation
- Multi-board analysis allows simulation of complete signal path across multiple board and substrate designs
- Extensive sweep simulation capability for virtually any trace parameter
- Random and user-defined data pattern stimulus for inter-symbol interference (ISI) analysis
- No limit to the number of simultaneous simulations
- Same environment for both simulation and layout
- Direct model binding and extraction to and from PCB Layout
- Ability to generate IBIS models from custom silicon models
- Source designs can be in Cadence or Mentor Graphics formats

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If you would like more information on PCB design or signal integrity please contact:

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