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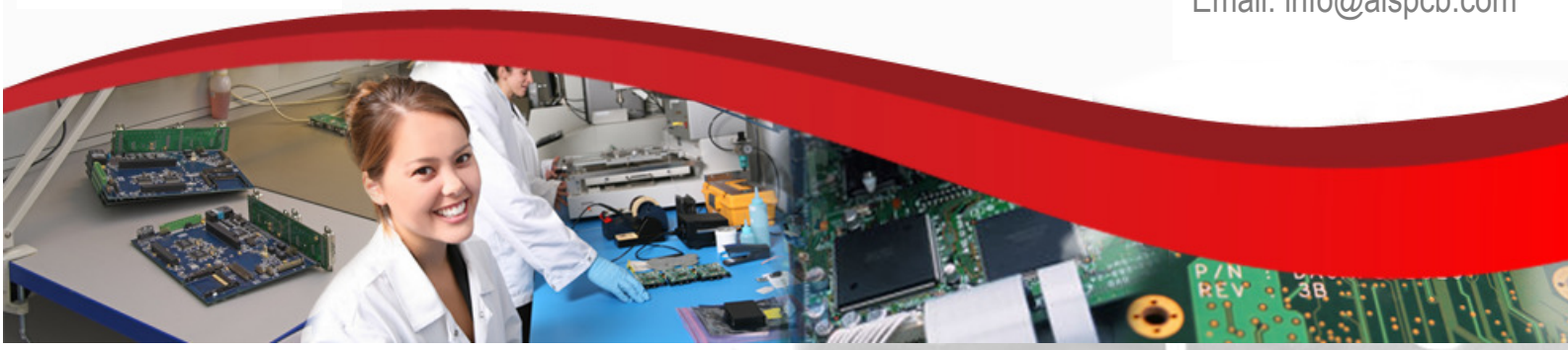

Current Thinking…

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Do you consider signal currents when designing terminations?

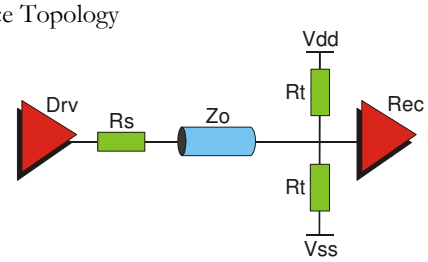
Signal currents are often overlooked when designing PCB interconnects and termination schemes. One reason why this may be the case is that voltages are generally of most concern to us; a signal's ability to satisfy the required VIL and VIH levels at the correct time is the extent of how we often gauge successful signalling. Another reason is that it's hard to measure current flow. Using an oscilloscope, signal voltages are easily studied by roaming the printed circuit board for pins, vias and test points on which to probe. Hardware is usually designed to make this as pain-free as possible, offering test access to all likely signals and ensuring that you are never far from a good ground connection. In contrast, hardware is almost never designed with 'ease of current measurement' in mind. Such measurements are usually a pain to take on existing hardware, generally requiring the signal path to be intercepted by cutting traces or lifting component pins.

Whatever the reasons for not looking closely at current flow, an increasing number of engineers are being forced to give it more thought in order to avoid simultaneous switching issues from large $\delta i/\delta t$ figures. Aside from signal integrity concerns, we are seeing customers increasing their effort to limit IO current purely to control power consumption, something especially true with hand-held and mobile product designers.

Fortunately, the SI tools used at Advanced Layout Solutions allow ***current-probing***, a feature omitted from most "IBIS-style" signal integrity simulators. This feature allows the current to be measured at any point in the signal path and provides our customers with current waveforms to accompany their voltage measurements. These waveforms can reveal problem areas that would never be detected by looking at voltage waveforms alone. For example, an unwanted situation such as ESD diode conduction can be clearly seen in current waveforms, yet is not apparent in v/t plots.

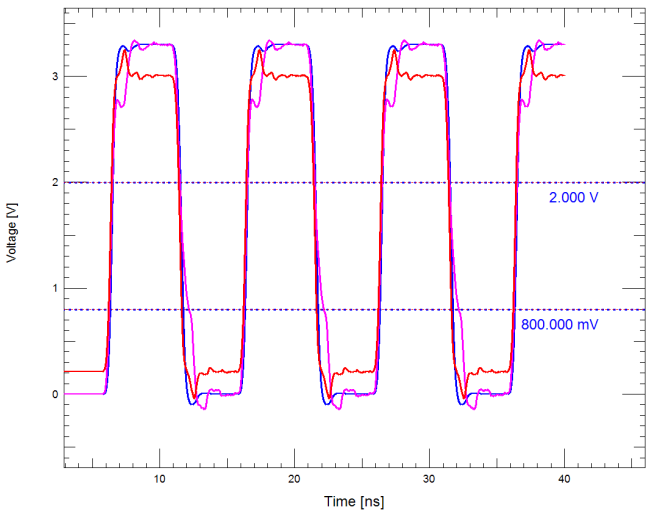
Figure 1 shows a simple topology in which three parameters can be varied: Rs – the resistance of a source series termination, Zo – the characteristic impedance of the signal path and Rt – the resistance of the end terminations to ground.

Figure 1. Trace Topology



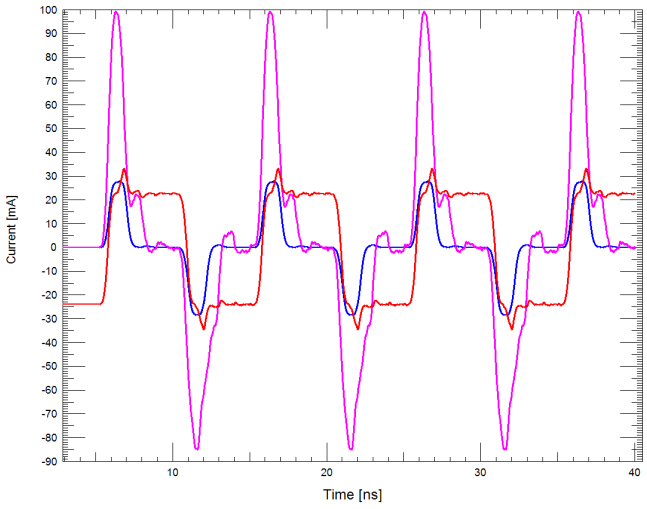
It is possible to achieve acceptable signalling waveforms with numerous combinations of these parameters. This is demonstrated in figure 2, in which three very different combinations all yield acceptable signals at the receiver… ***when only voltage is considered!***

Figure 2. Voltage Waveforms



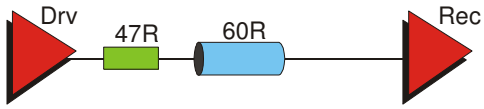
These three signals all have a similar rise-time, have good amplitude and are monotonic. Looking at voltage alone, nothing seems out of the ordinary. The truth is, however, that there are three very different topologies at work here, with the wildly different current flows shown in figure 3.

Figure 3. Current Waveforms



The red waveforms represent a far more familiar approach: parallel end-termination. In this scenario the trace has a characteristic impedance of 60-Ohms and is terminated to the supply rails with two 120-Ohm resistors. This style of termination gives very good signal quality but carries the overhead of significant quiescent current flow during times when the line is static.

Blue Topology



The blue waveforms represent source-termination. In this case a 60-Ohm transmission line is matched to the diver's output impedance using a 47-Ohm series resistor. For point-to-point, unidirectional signals this arrangement is ideal. Current only flows during propagation and there is no quiescent current flow during periods of inactivity.

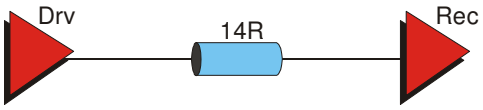
Source termination provides 'cleaner' waveforms than end-termination. This is because it gives a better match between Zo and the (small) driver inductance than end-termination gives between Zo and the (significant) load capacitance.

The current drive in a source-terminated line is generally thought to be less than that in an end-terminated line: a 'rule-of-thumb'. This is not necessarily correct. The *maximum* drive current in a source-terminated line is no different to that when using end-termination (biased midway). This current requirement exists during the round-trip propagation delay of the source-terminated line. However, in contrast to end termination the current returns to a negligible value after the round-trip is complete. This can be seen in figure 3 when comparing the red and blue waveforms.

There are many factors that influence the type of termination used on high-speed signals, not least are available board space and cost. But with the number of IOs utilised on today's systems increasing all the time, signal currents should be added to that list.

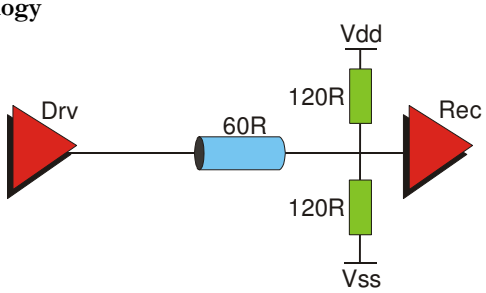
When running pre-route simulations to optimise your new IO design, make sure you use ***current probing*** *to get the whole picture!*

Magenta Topology



The magenta waveforms in figures 2 and 3 represent an unterminated topology with a transmission-line impedance matched to the output impedance of the driver (~14-Ohms). This seems like a great idea… until you see the excessive amount of current that this draws from the driver. Despite the associated high power-transients, ground-bounce and EMI levels, customers occasionally specify schemes such as this, and the large trace widths make them very unpopular with the layout designer!

Red Topology



If you would like more information on PCB design or signal integrity analysis please contact:

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