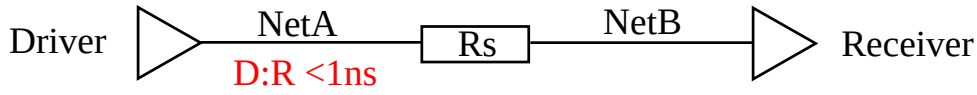
xNet Based Constraints Using OrCAD Capture (Allegro Design Entry CIS)

Problem Statement

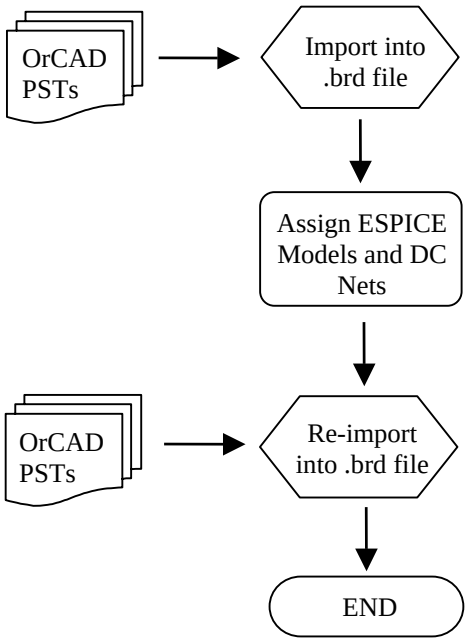
When assigning constraints in OrCAD Capture the "Driver/Receiver" style of pin-pair description may not create the correct pin-pairs in Allegro PCB if passive elements exist in the net topology. The simplest example is shown below:



In this topology the "*Driver/Receiver delay of less than 1ns*" constraint that is applied to NetA will not be applied across the full extent of the signal path as NetA and NetB are treated as two separate nets in OrCAD, with no relationship between them. When imported into Allegro PCB, the constraint will be converted to a pin-pair rule between the driver and resistor only. This is not the intention of the applied constraint.

Solution

The flow chart on the right shows the solution to this problem. In order to import the constraints correctly the PST files that are output from OrCAD must be imported into Allegro twice, once to initially import the logic and again AFTER the passive (ESPICE) models have been generated in Allegro PCB 610 or Allegro SI. Once these models have been generated, groups of nets connected together by passive elements will become extended nets, or *xNets*. Re-importing the PST files a second time will apply the OrCAD constraints to a board design with xNet connectivity. This will allow the "Driver/Receiver" constraints to map across the entire xNet and control delays between the correct pin-pairs. Note: all other constraint information applied in Allegro will be preserved when the new PST files are imported. New PST files may be repeatedly imported during layout but models must be generated for any new passive components for which this problem applies. **Care must be taken when deleting the incorrect pin-pair constraints that were created on the initial PST file import!**



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