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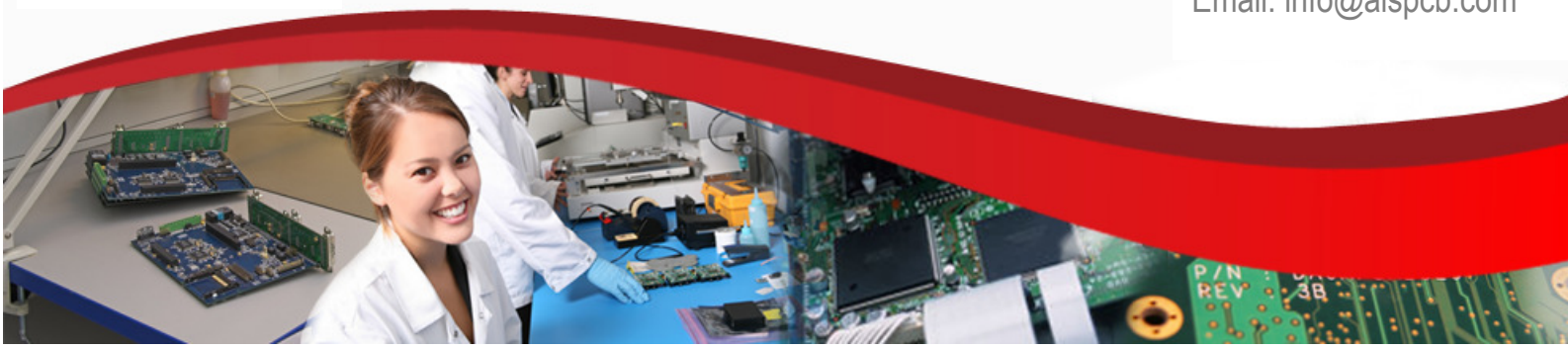

Successful Design With FPGA Transceivers

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Xilinx RocketIO™ & Altera HSSIO,

Advanced Layout Solutions Ltd provides the complete PCB design solution for your MGHz serial links.

There is a plethora of serial I/O standards emerging in the market today: PCI Express™ (formerly 3GIO), Fibre Channel, Serial RapidIO®, SerialLite, InfiniBand™, Gigabit Ethernet… the list goes on. All these protocols have one thing in common - they are based on high-speed differential signalling in the MGHz (Multi-GigaHertz) range, typically employing bit-rates from 1.25Gbps to 3.125Gbps.

The good news for hardware designers is that FPGA giants Xilinx and Altera have done the bulk of the design work for us, integrating high-speed serialiser/deserialiser (SERDES) I/Os into their devices to support these new standards. Altera provides a high-speed serial solution through its **Stratix™ GX** family of devices (HSSIO) and Xilinx through its **Virtex-II Pro** (RocketIO™). Each of these provides multiple 3.125Gbps transceivers channels, the characteristics of which can be controlled in software via user - programmable gain, pre-emphasis and termination settings.

So, with the difficult bit already done for us, do we simply connect the devices together at the PCB level? Not quite. As you would expect, altering the programmable settings has a significant impact on the eye diagrams. However, it is quite remarkable how much the data eye changes as physical interconnect properties, such as impedance and Er, are varied. Alarmingly, the difference between a robust MGHz link and a poor, error prone one can be as little as a differential impedance mismatch or presence of an inadequate connector.

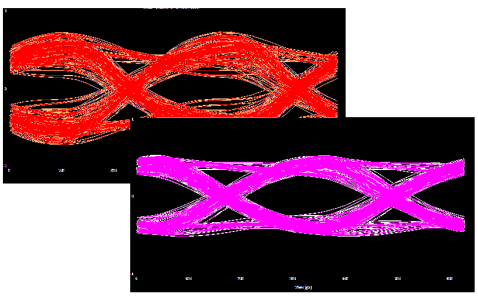

Fig1. Altera HSSIO DML simulations showing effect of varying link differential impedance.

How can ALS help?

As a bureau, Advanced Layout Solutions Ltd (ALS) is exposed to a wide range of hardware designs. We are currently seeing an increasing number of our clients taking advantage of the 'off the shelf' MGHz FPGA offerings, in fact, the majority of designs that come through our offices now have high-speed differential pairs of some description on them. However, we are also seeing an increase in new clients coming to us with problematic high-speed serial links.

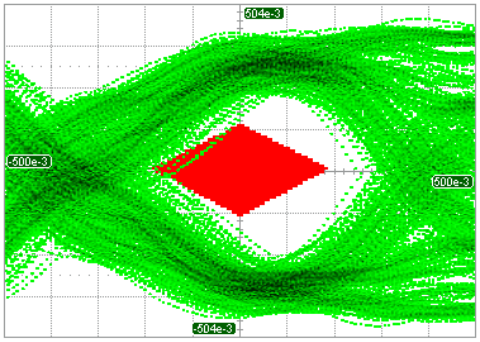

Fig2. Compliance eye showing mask violations - with so little room for error we must design every section of MGHz interconnect with care.

Why should this be the case? Probably because with the shift from parallel bus structures to serial links must come a corresponding shift in design methodology. There are just as many PCB constraints to control with a serial link, but they differ from those involved in parallel structures. Where we may previously have gone to great lengths to control propagation delay between bits of a bus, we must now turn our attention to impedance continuity and dielectric losses.

Simulation and constraint-driven layout are the keys to successfully designing-in MGHz serial links. These links operate on the edge of functionality - in order to transfer data at such a high rate protocols expect *some* errors and consider a small error rate to be within specification. Operating with such a small amount of headroom in this way means it is often the case that even small improvements to the PCB interconnect will make the link far more robust.

Board-Level Simulation

The starting point in MGHz link design is pre-route simulation, the results of which yield a set of design constraints. Once these constraints have been identified they will be used to drive the layout process, ensuring that the completed routing performs as expected. The constraints will take the form of a set of rules that the routing must obey, such as trace length, width, impedance, etc. To determine what these constraints should be requires multiple simulations to be run and the impact on the eye diagram observed. These simulations are run in sweep batches whereby the simulator will run multiple simulations whilst varying a parameter, or combinations of parameters. But the results of these (and any other) simulations are only as good as the models used. For this reason the interconnect is modelled with all frequency dependant phenomena, such as skin effect and dielectric heating loss, taken into account. If you are under the illusion that you can simulate your MGHz link with a standard differential IBIS model… you're wrong! An IBIS model describes the behaviour of a driver's rising and falling edges. Serial transceivers have data-dependant output characteristics such as 'pre-emphasis' that places them well out of the reach of the current IBIS specification. As we are going to make engineering decisions based upon the simulation results, we need them to be as accurate as possible. For this reason we need 'golden' models that the vendor claims are not only accurate, but are also verified against their real-world silicon. That's exactly what Advanced Layout Solutions have from both Altera and Xilinx. At ALS we use the Cadence Allegro tool set in conjunction with both Cadence's **'tlsim'** and Synopsys's **'HSPICE®'** simulators to ensure the most accurate simulation environment available. For Altera's Stratix™ GX devices we use Cadence's Device Modeling Language (DML) models that fully describe the behaviour of the transceiver. For the Xilinx RocketIO™ we use verified encrypted HSPICE® transistor-level models. Furthermore, Allegro® PCB SI™ gives us the ability to simulate across multiple PCBs (most commonly the backplane/plug-in card scenario) to ensure signal integrity across your whole system.

Configurable Transceivers

The table below shows the 'soft' settings available to the user for both the Xilinx and Altera transceivers. These same settings are programmable within the simulation models, allowing us to simulate the customer's exact implementation.

Parameter	Number of Settings
Pre-emphasis	Xilinx = 4, Altera = 6
Output Level	Xilinx = 5, Altera = 6
Tx Termination	Xilinx = 2
Rx Termination	Xilinx = 2
Rx EQ	Altera = 5

Table 1. Transceiver soft settings.

These settings yield 80 possible configurations for a Xilinx RocketIO™ and 180 for Altera's HSSIO. Although these configurable I/Os offer great flexibility they can also encourage a blasé attitude towards the design of the physical interconnect, as they give the engineer a potential 'safety net', whereby there are plenty of settings to fiddle with when the design doesn't operate as hoped. If a MGHz serial link has poor interconnect it is unlikely that adjusting the soft settings will achieve a satisfactory result; the soft settings are there for fine-tuning, **not repair!**

Parameter	Settings
Differential Impedance	∞
Impedance continuity (necking etc)	∞
Trace width (linear resistance)	∞
Trace length (line loss)	∞
Differential pair phase alignment	∞
Dielectric Constant (Er)	∞
Dielectric Loss Factor (tan δ)	∞

Table 2. Physical interconnect parameters.

By comparison, the table above shows the key parameters that can be adjusted by physical interconnect design. Do not underestimate the significance of these parameters with respect to the performance of the link. It may be the case that each only contributes a small amount of signal distortion, but the aggregate effect can be dramatic. Fig3 demonstrates this fact - in this Xilinx example refining a number of interconnect properties has opened up the data eye three-fold.

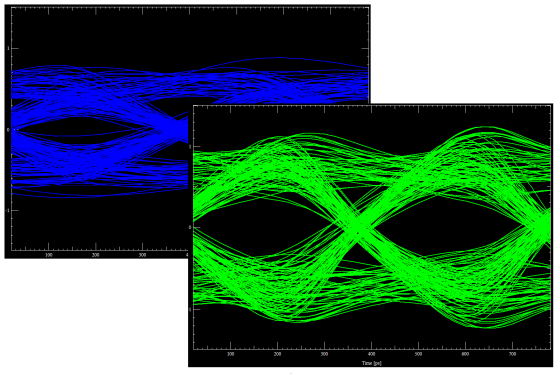

Fig3. Xilinx RocketIO™ HSPICE® simulation. The vertical opening is increased 3x by PCB design alone.

Conclusion

Serial MGHz links are continuing to increase in both popularity and bit rate. Altera's new Stratix™II GX chips use 6.5Gbps I/Os and Xilinx's Virtex-4 devices feature a RocketIO™ transceiver capable of over 10Gbps. The design challenges at the PCB level associated with these technologies are therefore only going to get more complex. To ensure the minimum number of board re-spins, and thus the shortest time to market, it is essential that board-level simulation be carried out on your MGHz serial links.

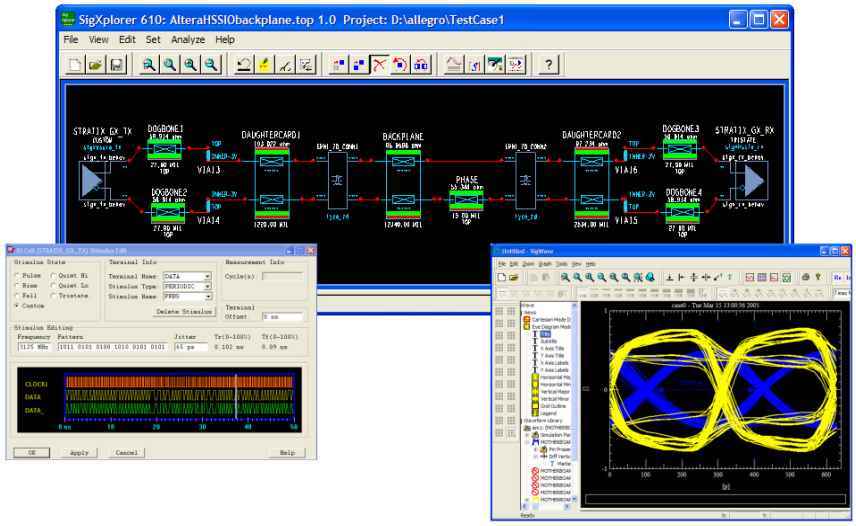

Fig4. "Allegro® PCB SI™ - proactively addresses issues typical of 3.125-Gbps links."

"Our customers' ability to quickly design-in the Virtex-II Pro RocketIO™ technology is critical. Working with Cadence, we are minimizing the design-in time for our customers, enabling them to take advantage of dramatic system cost savings through the implementation of the serial technology in their next design."

Rich Sevcik – Xilinx, Inc.

"By delivering the first fully behavioural SERDES model, Altera customers implementing Stratix GX devices are able to proactively address link simulation issues typical of 3.125-Gbps transceiver designs. In Allegro® PCB SI™, our behavioural DML model performs at least 20 times faster than traditional transistor-level models without sacrificing accuracy."

Vipul Badoni – Altera, Inc.

If you would like more information on MGHz links, PCB design or signal integrity please contact:

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